FIG. 1

FPGA blocks for User-specific functions and I/O interfaces

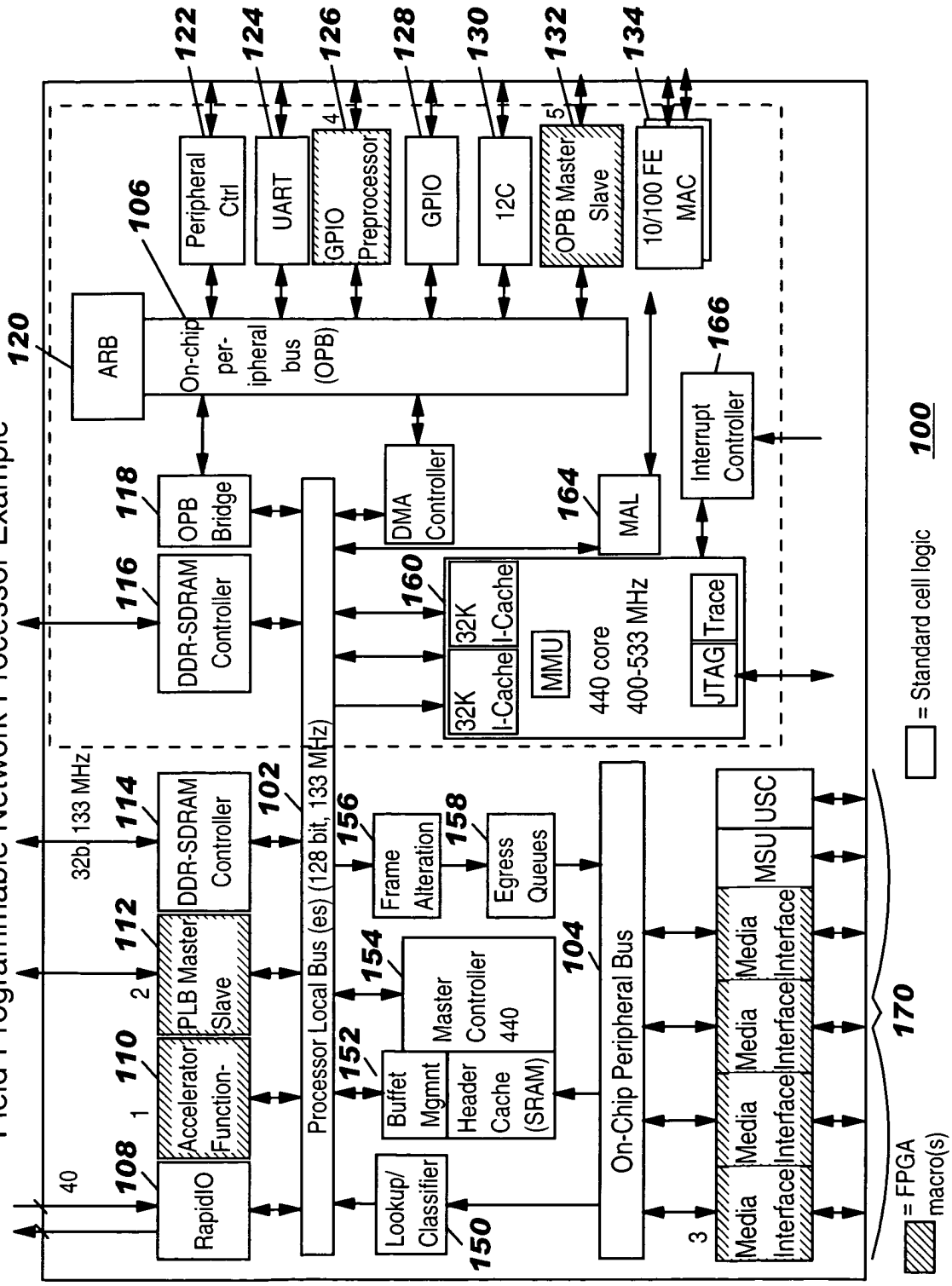


FIG. 2

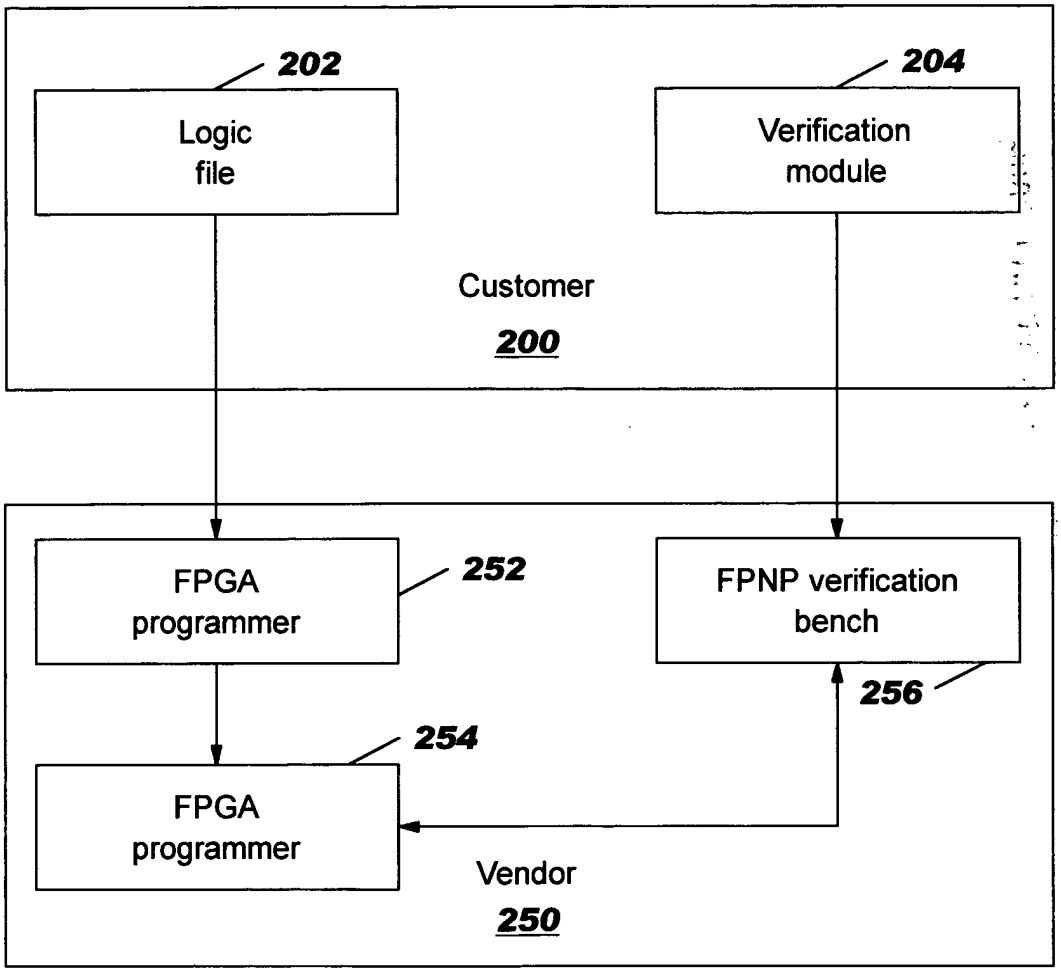
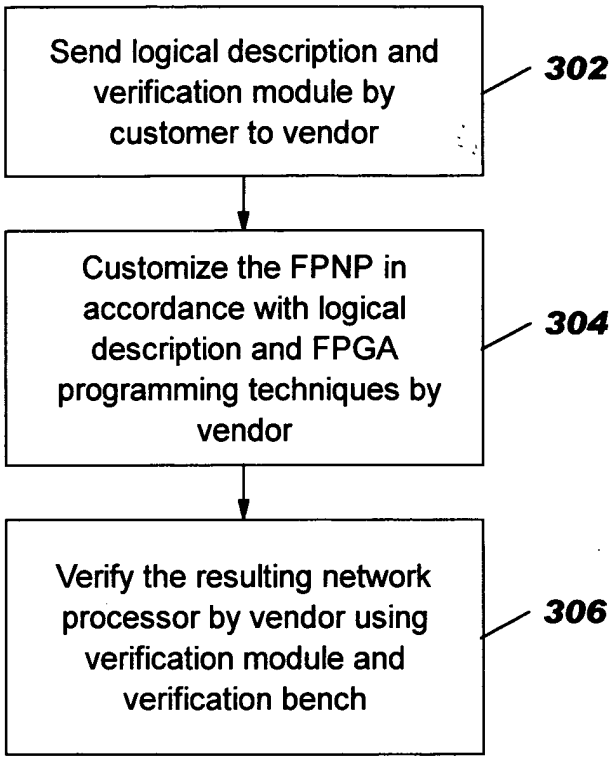

202
Logic file
204
Verification module
Customer
200
FPGA programmer
252
FPNP verification bench
256
254
FPGA programmer
Vendor
250

FIG. 3


Send logical description and verification module by customer to vendor
302
Customize the FPNP in accordance with logical description and FPGA programming techniques by vendor
304
Verify the resulting network processor by vendor using verification module and verification bench
306